ABSTRACT OF THE DISCLOSURE

A low voltage of the order of or one to three volts instead of an intermediate V_{PASS} voltage (e.g. of the order of five to ten volts) is applied to word line zero immediately adjacent to the source or drain side select gate of a NAND flash device to reduce or prevent the shifting of threshold voltage of the memory cells coupled to word line zero during the programming cycles of the different cells of the NAND strings. This may be implemented in any one of a variety of different self boosting schemes including erased areas self boosting and local self boosting schemes. In a modified erased area self boosting scheme, low voltages are applied to two or more word lines on the source side of the selected word line to reduce band-to-band tunneling and to improve the isolation between two boosted channel regions. In a modified local self boosting scheme, zero volt or low voltages are applied to two or more word lines on the source side and to two or more word lines on the drain side of the selected word line to reduce band-to-band tunneling and to improve the isolation of the channel areas coupled to the selected word line.